Primary Side Quasi-Resonant BJT Controller with CV/CC Operation

REV. 00

General Description

The LD7515A is an excellent primary side feedback BJT controller with CV/CC operation, integrated with several functions of protections. It minimizes the component counts and is available in a tiny SOT-26 package. Those make it an ideal design for low cost applications.

It provides functions of ultra-low startup current, green-mode power-saving operation and leading-edge blanking of the current sensing. Also, the LD7515A features Internal OTP (Over Temperature Protection) and OVP (Over Voltage Protection) to prevent the circuit from being damaged due to abnormal conditions.

In most cases, the power supply with primary-side feedback controller would accompany with some serious load regulation effect. To deal with this problem, the LD7515A consists of dedicated load regulation compensation circuit to enhance its performance.

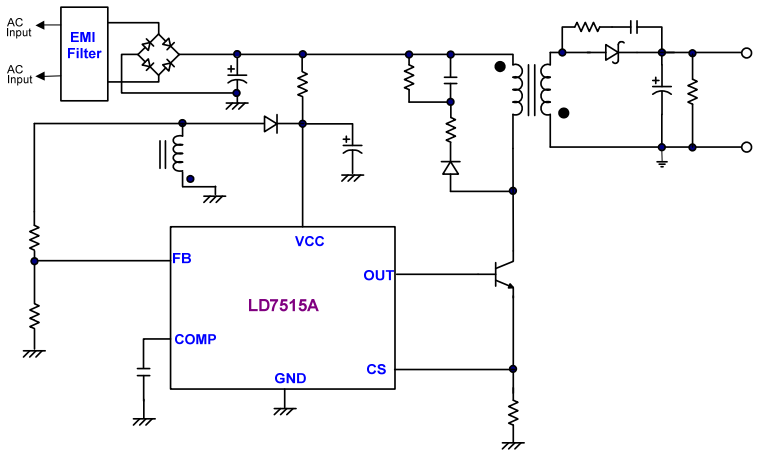
Features

- Primary-Side Feedback Control with Quasi-Resonant Operation
- Direct Drive of BJT Switch
- Constant Voltage within ±5%
- Built-In Adjustable Load Regulation Compensation
- Constant Current Control
- Ultra-Low Startup Current (<1.9μA)
- 0.5mA Low Operating Current at Light Load
- 75 kHz Maximum Switching Frequency.
- Current Mode Control
- Green Mode Control Improve Efficiency
- LEB (Leading-Edge Blanking) on CS Pin
- Built-in Soft Start
- VCC OVP (Over Voltage Protection)
- FB Pin Open/Short Protection
- Internal OTP (Over Temperature Protection)

Applications

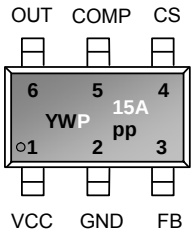
- Mobile Phone Charger
- Lower Power AC/DC Adapter

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
P15A : LD7515A

Ordering Information

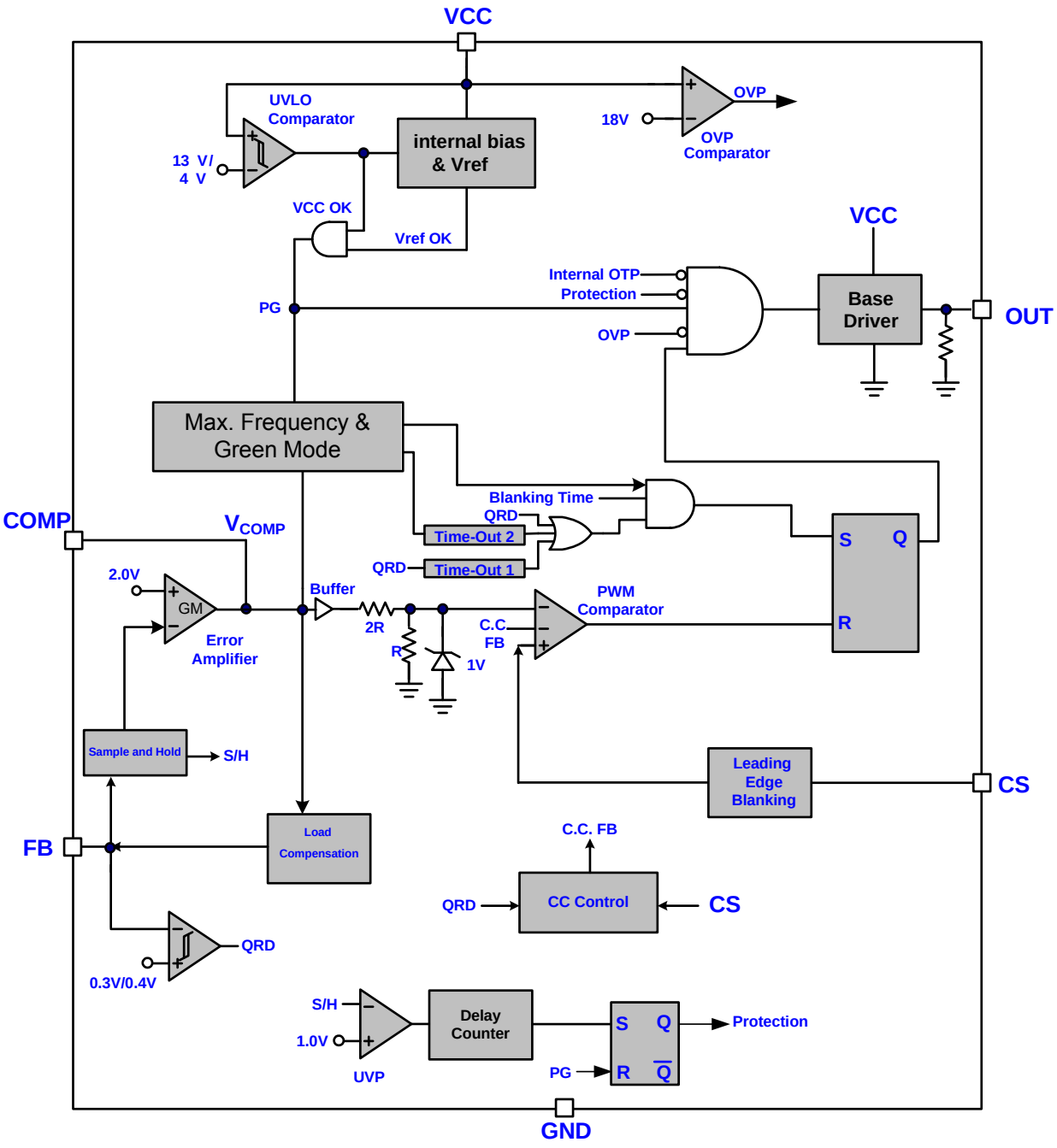
Part number	Package	Top Mark	Shipping
LD7515A GL	SOT-26	YWP/15A	3000 / tape & reel

The LD7515A is ROHS compliant / Green Packaged

Pin Descriptions

PIN	NAME	FUNCTION
1	VCC	Supply voltage pin.
2	GND	Ground.
3	FB	Auxiliary voltage sense and Quasi Resonant detection.
4	CS	Current sense pin, connect to sense the Switch current.
5	COMP	Output of the error amplifier for voltage compensation.
6	OUT	Base drive output to drive the external BJT Switch.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	20V
OUT	-0.3V ~ 3.3V
COMP, FB, CS	-0.3V ~ 3.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	200mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Ambient Temperature	-40	85	°C
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	4.8	16	V
VCC Capacitor	1	10	μF
Start-up resistor Value (AC Side, Half Wave)	1M	6.6M	Ω
Comp Pin Capacitor	470	4700	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12.0V)

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC=UVLO(ON) – 50mV	I_{CC-ST}		1.0	1.9	μA
Operating Current	V_{COMP}=0V, OUT=open, FB=2V	I_{CC-OP2}	0.4	0.5	0.6	mA
	OVP/FB UVP tripped, FB=0V	I_{CC-OPA}	0.18	0.25	0.32	mA
UVLO (OFF)		V_{CC-OFF}	3.4	4.0	4.6	V
UVLO (ON)		V_{CC-ON}	12	13	14	V
VCC OVP Level		V_{CC-OVP}	17	18	19	V
Error Amplifier (COMP pin)						
Reference Voltage, V_{REF}		V_{REF}	1.98	2.00	2.02	V
Transconductance		gm-comp		85μ		1/Ω
Output Upper Clamp Voltage	V_{FB}=1V	$V_{COMP-CLAMP}$	2.8	3.0	3.2	V
Load Compensation Current	V_{COMP}=3V	I_{LOAD_Comp}	17	20	23	μA
Current Sensing (CS Pin)						
Maximum Input Voltage, V_{CS-OFF}		V_{CS-MAX}	0.93	1	1.07	V
Minimum V_{CS-OFF}	V_{COMP} < 0.45V	V_{CS-MIN}	0.135	0.15	0.165	V
Leading Edge Blanking Time		T_{LEB}	530	650	770	ns
QRD (Quasi Resonant Detection, FB Pin)						
QRD Trip Level	*	V_{QRD}		300		mV
	Hysteresis*	$V_{QRD-HYS}$		100		mV
Oscillator for Switching Frequency						
Maximum Frequency		F_{SW-MAX}	69	75	81	kHz
Green Mode Frequency		$F_{SW-GREEN}$		25		kHz
Minimum Frequency		F_{SW-MIN}	0.83	1.2	1.47	kHz
Output Drive (OUT Pin)						
Max. Output Base Current	VCS=1V	I_{B-MAX}	55	60	69	mA
Maximum On Time		T_{ON-MAX}	10	13	18.5	μs
FB Under Voltage Protection (UVP, FB Pin)						
Under Voltage Level		V_{FB-UVP}	0.9	1.0	1.1	V
UVP Delay Time	After soft start*	$T_{D-FBUVP}$		10		ms
On Chip OTP (Over Temperature)						
OTP Level	*	T_{INOTP}		140		°C
OTP Hysteresis	*	$T_{INOTP-HYS}$		15		°C

*: Guaranteed by design.

Typical Performance Characteristics

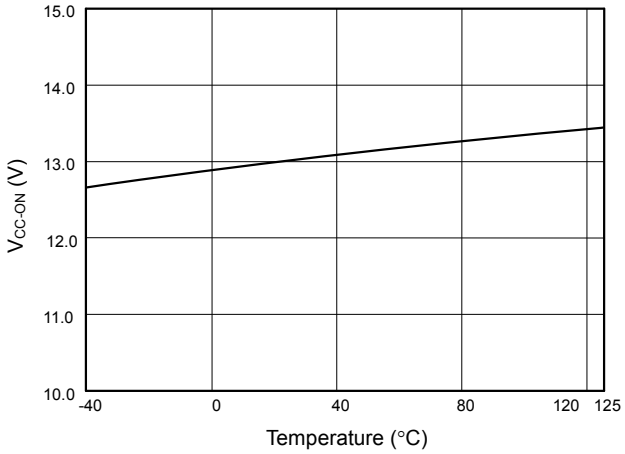


Fig. 1 UVLO(ON) vs. Temperature

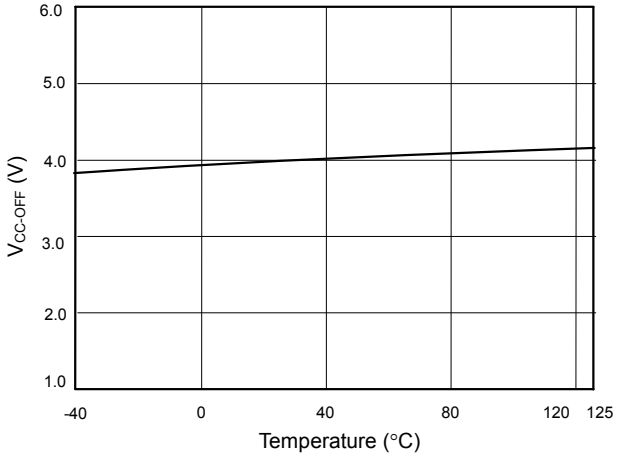


Fig. 2 UVLO(OFF) vs. Temperature

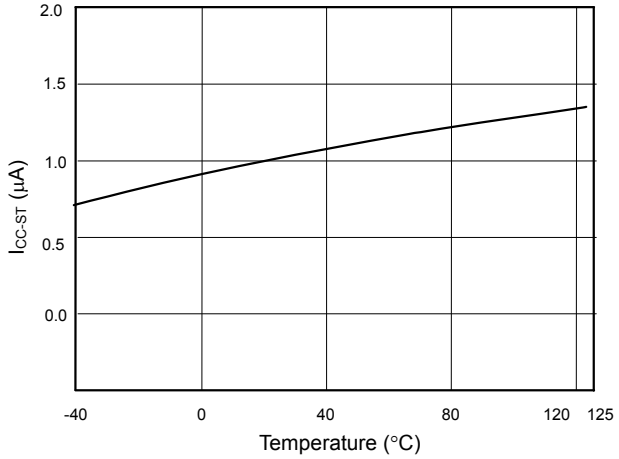


Fig. 3 Startup Current vs. Temperature

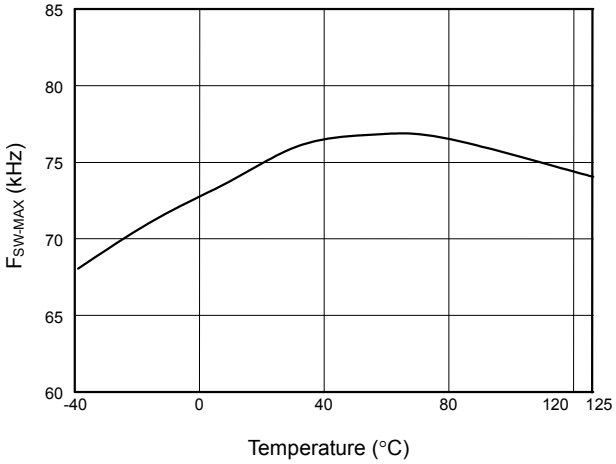


Fig. 4 Max Frequency vs. Temperature

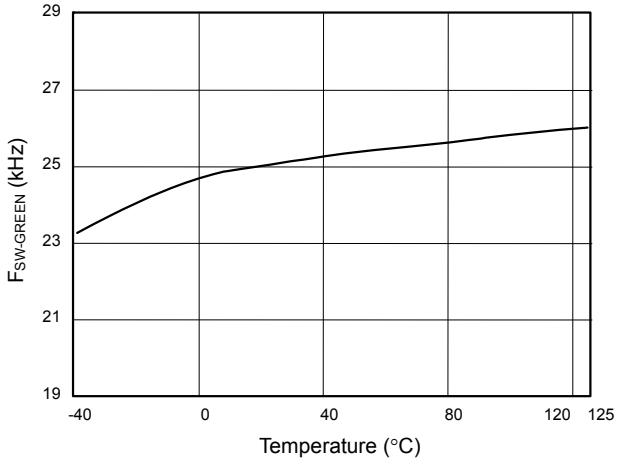


Fig. 5 Green Mode Frequency vs. Temperature

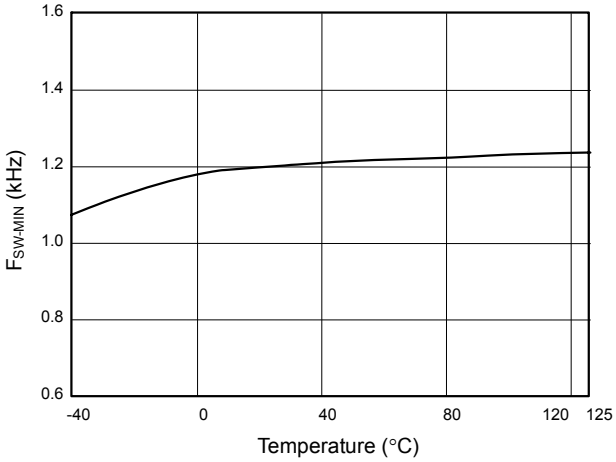


Fig. 6 Min Frequency vs. Temperature

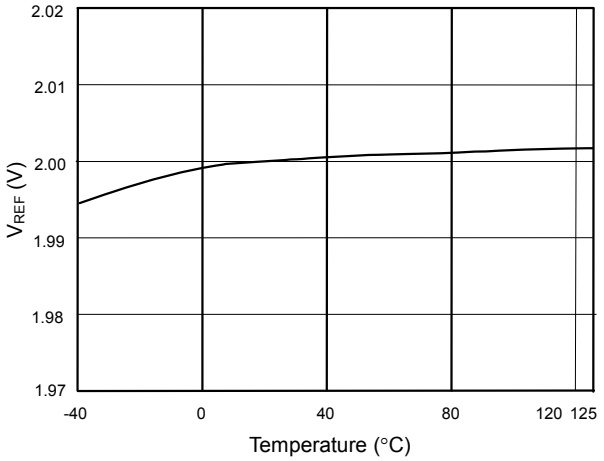


Fig. 7 Reference Voltage vs. Temperature

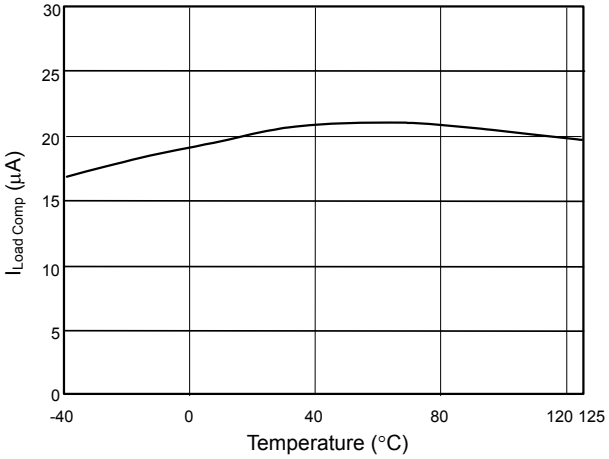


Fig. 8 Load Compensation vs. Temperature

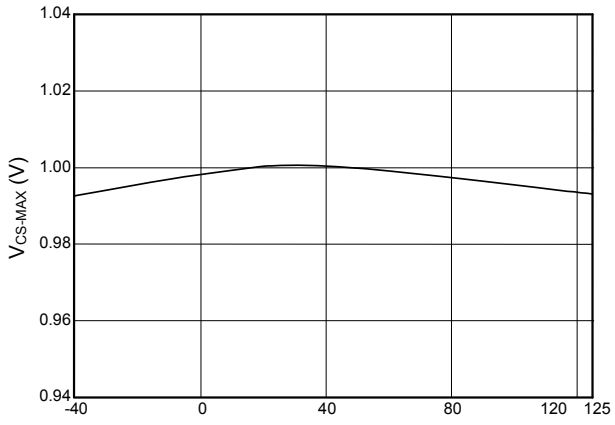


Fig. 9 V_{CS} (off) vs. Temperature

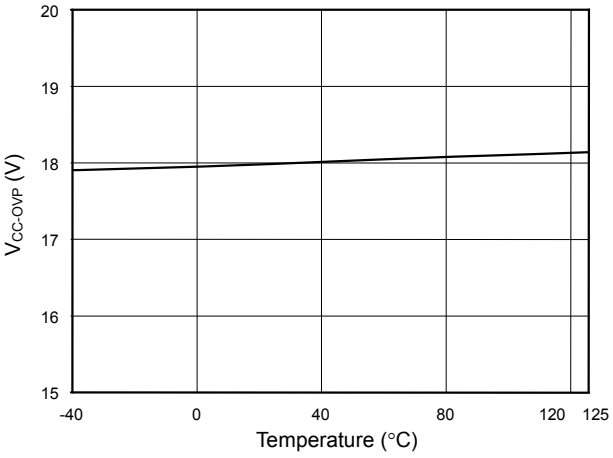


Fig. 10 VCC OVP vs. Temperature

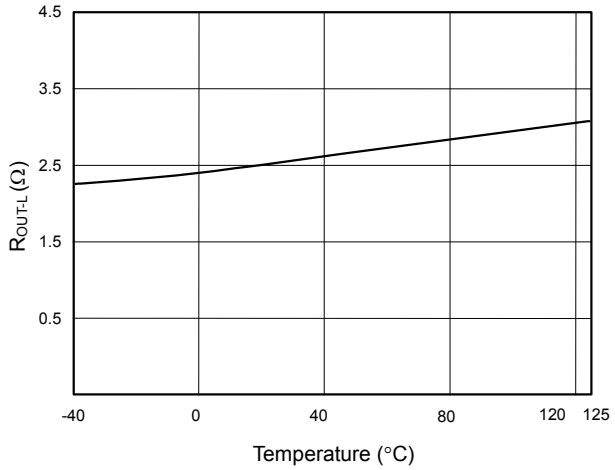


Fig. 11 Output Low ON-resistance vs. Temperature

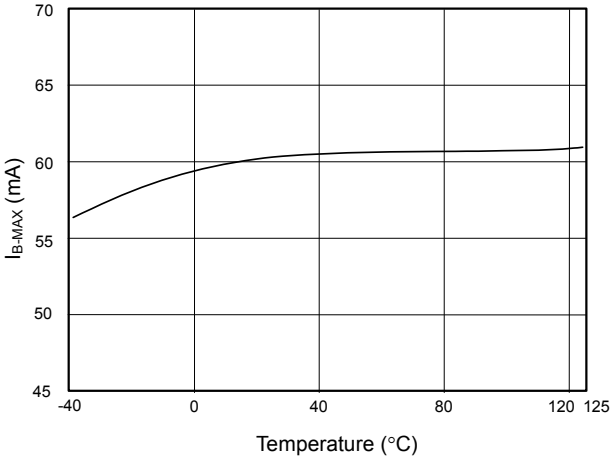


Fig. 12 Max. Output Base Current vs. Temperature

Application Information

Operation Overview

The LD7515A is an excellent primary side feedback controller with Quasi-Resonant operation to provide high efficiency and better EMI performance. The LD7515A removes the need for secondary feedback circuits while achieving excellent line and load regulation. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrates with more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD7515A PWM controllers and further to drive the power BJT. As shown in Fig. 13, a hysteresis is built in to prevent shutdown from voltage dip during startup.

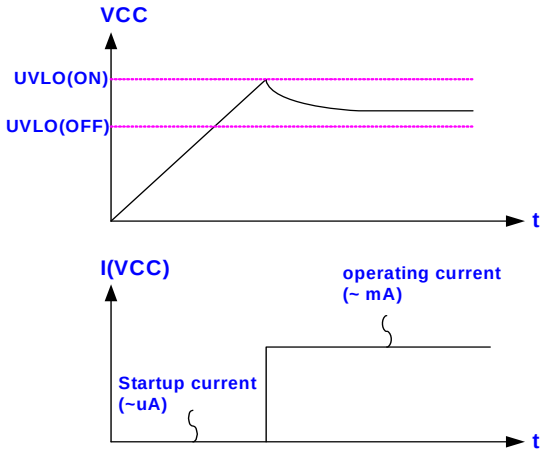


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD7515A is shown in Fig. 14. During startup transient, the VCC sinks below the UVLO threshold, so there's no pulse delivering out from LD7515A to drive the power BJT. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to enable the LD7515A to deliver the drive-out signal, the auxiliary winding will provide the supply current instead. If PWM controller requires less current to start up, it will allow less power consumption on R1. By using CMOS process and some unique circuit design, the LD7515A requires only 1.9μA max to start up. Higher resistance of R1 will spend much more time to start up. The user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

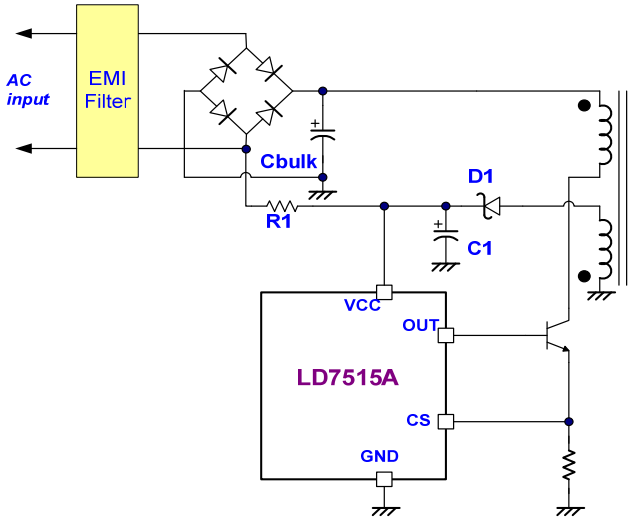


Fig. 14

Principle of CV Operation

In the DCM Flyback converter, it senses the output voltage by auxiliary winding. LD7515A samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 15. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the BJT is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time and will be hold until the next sampling. The sampled voltage is compared with internal reference V_{REF} (2.0V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.0V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_F$$

Where V_F indicates the drop voltage of the output Diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the collector voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 16 shows the desired collector voltage waveform in compare to those with large undershoot due to leakage inductance induced ring (Fig. 17). This will make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor RS, in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 18.

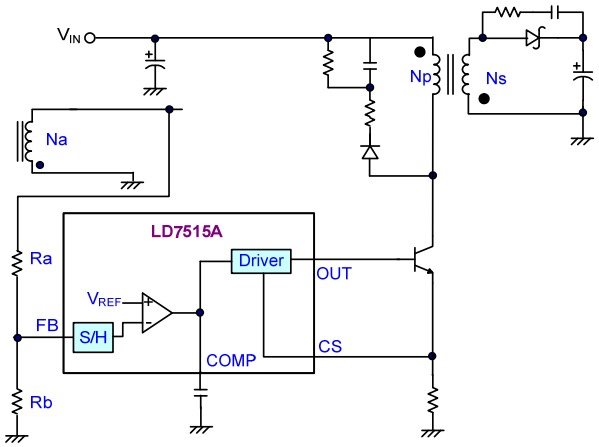


Fig. 15

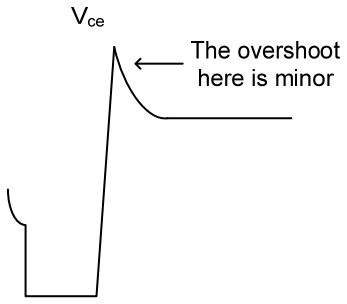


Fig.16

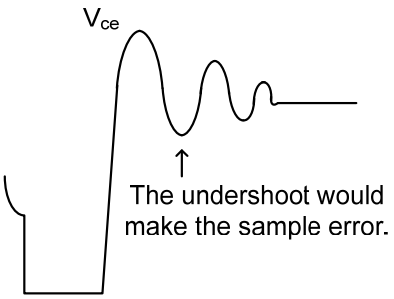


Fig.17

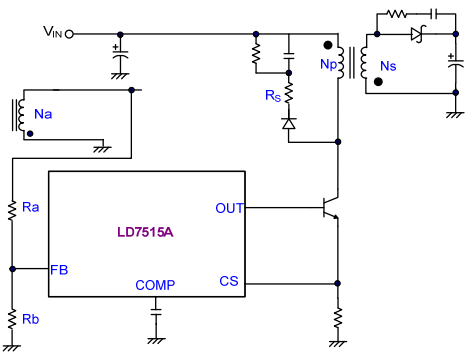


Fig.18

Load Regulation Compensation

LD7515A implements with load regulation compensation to compensate the cable voltage droop and to achieve a better voltage regulation. The offset voltage is created across FB by an internal sink current source which feeds out the FB during the sampling period. The internal sink current source is proportional to the value of V_{COMP}, as shown in Fig. 19. As a result, the drop due to the cable loss can be compensated. So, the offset voltage decreases as the V_{COMP} decreases in condition from full-load to no-load. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. The equation of internal sink current source is shown as:

$$I_{FB} = (V_{COMP} - 0.45) * 7.84 \quad (\mu A)$$

The maximum compensation is shown as:

$$\frac{\Delta V}{Vo} = \frac{I_{FB} \times (Ra \;//\; Rb)}{2}$$

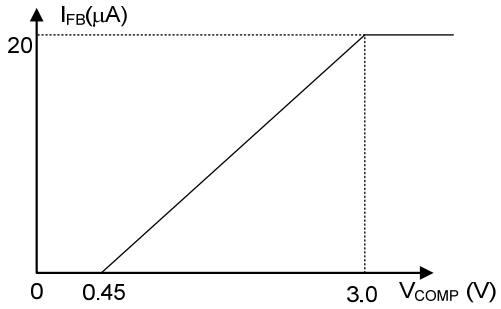


Fig. 19

Quasi-Resonant Mode Detection

The LD7515A employs quasi-resonant (QR) switching scheme to switch valley-mode either in CV or CC operation. This property feature greatly reduces the switching loss and dv/dt in the entire operating range for the power supply. Fig. 20 shows the typical QR detection block. The QR detection block will detect auxiliary winding signal to drive BJT as FB pin voltage drops to 0.3V. The QR comparator would not operate if FB pin voltage remains above 0.4V. The 4ms of time-out2 generates a BJT turn-on signal as the driver output drops to low level for more than 4ms with the falling edge of the driver output.

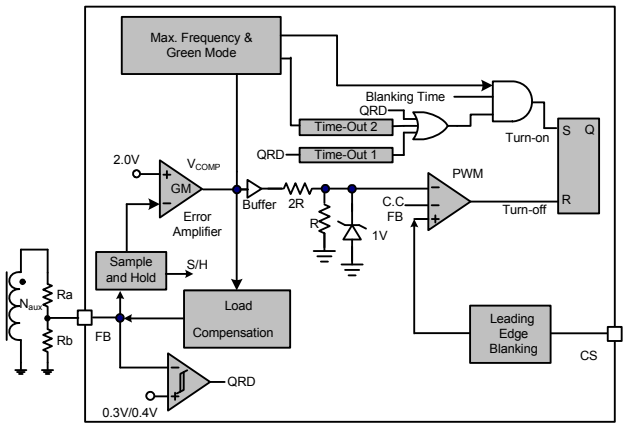


Fig. 20

Multi-Mode Operation

The LD7515A is a QR controller operating in multi-modes. The controller changes operation modes according to line voltage and load conditions. At heavy-load (V_{COMP}>1.5V, Fig. 21), there might be two situations to meet. If the system AC input is in low line, the LD7515A will turn on in first valley. If in high line, the switching frequency will increase till over the clamp of 75KHZ and skip the first valley to turn on in 2nd valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in QR mode.

At medium or light load conditions (1.1V<V_{COMP}< 1.5V, Fig. 15), the frequency clamp is reduced to 25 kHz maximum as V_{COMP} down to V_{SG1}. However, the valley switching characteristic behaves as well in these conditions. The LD7515A will jump to turn on in 3rd, 4th…. valley. That is, when load decreases, the system automatically skip more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold back is realized and high power efficiency is achieved.

At zero load or very light load conditions (V_{COMP}<0.7), the system operates in green mode for power saving. In green mode, the system modulates the frequency according to the load and V_{COMP} conditions. Once V_{COMP} is lower than V_{SG2}, the switching frequency starts to linearly decrease from 25 kHz to 1.2 kHz.

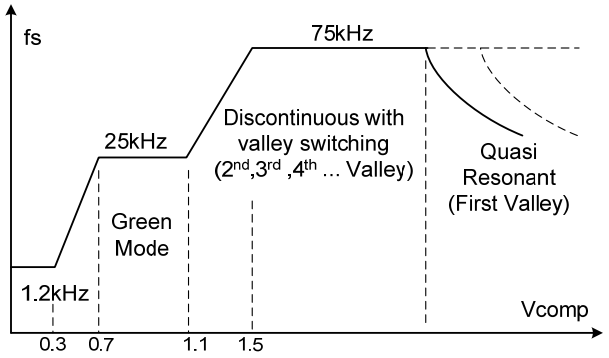


Fig. 21

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 22, the LD7515A detects the primary BJT current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1V. From above, the BJT peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{1V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

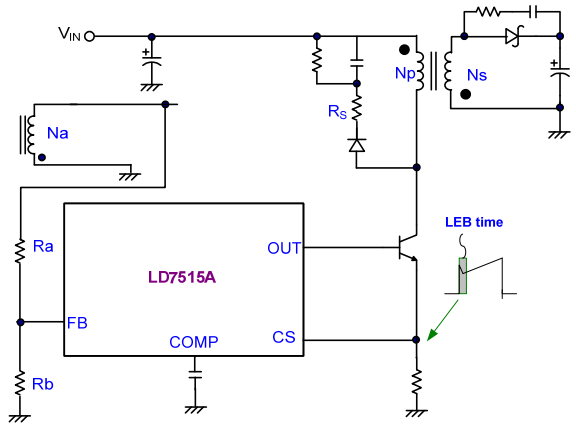


Fig. 22

Principle of C.C. Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 23. The output current Io can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{Ts}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$

The primary peak current $i_{P,PK}$, inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of V_{CS}*T_{DIS}/T_S will be modulated as a constant (V_{CS}*T_{DIS}/T_S =1/3). I_O can be induced finally by

$$Io \cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$
$$\cong \frac{1}{2}\frac{N_P}{N_S} \times \frac{1}{R_S} \times \frac{1}{3}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

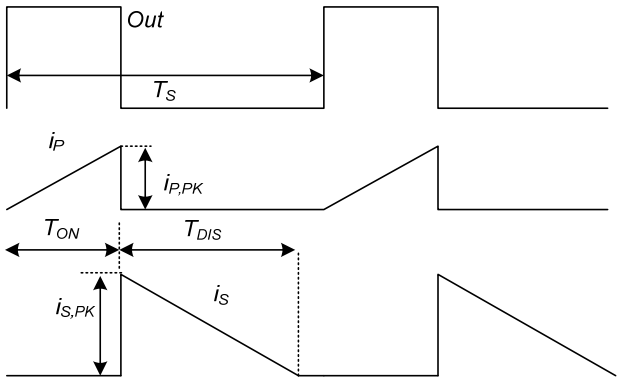


Fig. 23

OVP (Over Voltage Protection) on VCC – Auto Recovery

LD7515A is implemented with OVP function over VCC. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shutdown simultaneously thus to stop the switching of the power BJT until the next UVLO(ON) arrives. The VCC OVP function of LD7515A is an auto-recovery type protection. The Fig. 24 shows its operation. On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

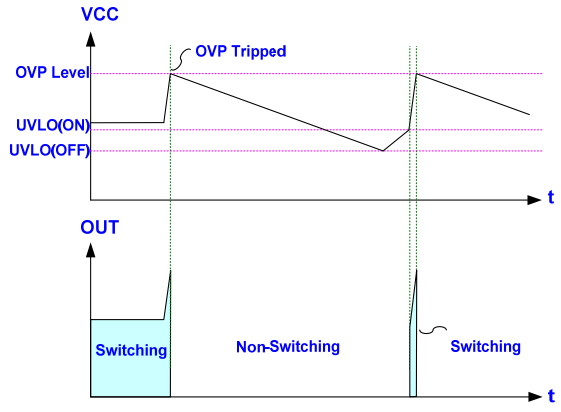


Fig. 24

FB Under Voltage Protection (FB UVP) – Auto Recovery

LD7515A is implemented with an UVP function over FB pin. If the FB voltage falls below 1.0V for over the delay time of FB UVP, the protection will be activated to stop the switching of the power BJT until the next UVLO(ON) arrives. The FB UVP function in LD7515A is an auto-recovery type protection. The Fig. 25 shows its operation. The FB UVP is disabled during the soft start.

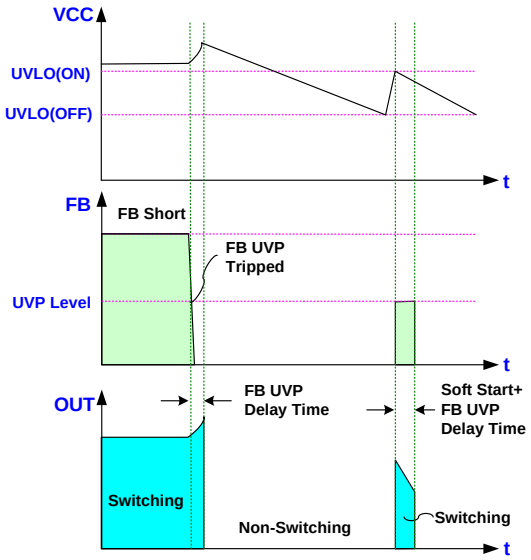
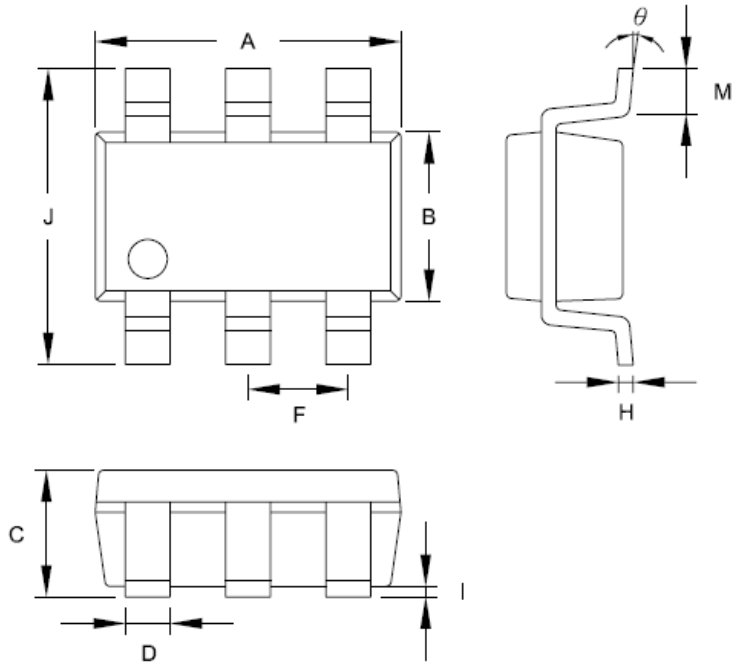


Fig. 18

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	07/02/2014	Original Specification.